MV3 - MARVELL MV64660 implementation

This course covers Marvell Discovery VI devices

Objectives

- The course describes the MV64660 internal data paths.
- The course explains how the host PowerPC and a CPU connected to PCI-X can synchronize to each other through the message unit.
- Operation of the PCI Express interface is detailed in Root Complex mode as well as in Endpoint mode.
- A long introduction to DDR SDRAM is done prior to describe the DDR SDRAM controller operation.
- The course focuses on the hardware implementation of the DDR SDRAM.
- The training explains how to implement chained DMA transfers, by using either IDMA channels or XOR engines.
- The course highlights the possible optimizations that can be implemented to boost the performance of the Ethernet controller.

A more detailed course description is available on request at training@ac6-training.com

Pre-requisites

- Knowledge of PowerPC 60X / MPX bus. See our courses on NXP and IBM Microelectronics PowerPCs.

Related courses

- Ethernet and switching, reference cours N1 - Ethernet and switching
- PCI express, reference cours IC4 - PCI Express 3.0
- USB Full Speed High Speed, reference cours IP2 - USB 2.0
- Serial-ATA, reference cours IS3 - Serial ATA III

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.

- En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

OVERVIEW

- 6-bus architecture, organization of a board based on MV64660
- Frequency domains, fast path between CPU and SRAM / SDRAM
- Data integrity checking
- Internal crossbar
- Master de-mux programming, address decode windows
- Slave mux programming, pizza arbiters operation

CPU INTERFACE

- CPU address space decoding
- CPU-to-PCI address remapping
- Protection windows
- Arbitration, multi-processor operation
- CPU slave operation
- Cache coherency
- Deadlock avoidance
- Transaction ordering
- Hardware implementation, clocking, low power modes

DDR2 INTERFACE

- Introduction to DDR SDRAM from Jedec specification
- DDR2 on-die terminations
- Clocking
- Initialization sequence
- Data synchronization : DQS signals, programmable DLL
- DDR2 SDRAM controller, functional description
- Page management
- Read and write transactions
- ECC and read-modify-write transactions
- Hardware implementation, ODT management (internal and external)
- Low power modes

DEVICE CONTROLLER

- Transaction queue, read and write data buffers
- Address and data multiplexing
- Timing parameters
- External acknowledgement
- Pack / unpack and burst support
- NAND flash support, boot from NAND flash

PCI INTERFACE

- PCI bus arbitration
- Master operation in PCI and PCI-X mode
- Target operation in PCI and PCI-X mode
- PCI-to-PCI configuration transactions
- Address decoding

PCI-EXPRESS x4 AND x1 INTERFACES

- Integrated low power SERDES PHY
- x1, x4 link
- Operating as either Root Complex or Endpoint
- Link initialization
- Arbitration and ordering
- Peer-to-peer traffic
- Messaging unit, synchronization between CPUs through PCI/PCI-Express

GENERAL PURPOSE INPUT/ OUTPUT PINS

- GPIO port, functional description
- Interrupt request inputs
- Multi Purpose Pin multiplexing

INTERRUPT CONTROLLERS AND TIMERS

- Watchdog timer
- Interrupt controller functional description
- Interrupt steering logic to 4 possible output pins
- Priority mechanism

TWSI CONTROLLER AND RESET

- Master and slave operation, 7- or 10-bit addressing
- Determining the current state of the controller by reading the status register
- Master write sequence, master read sequence
- Slave write sequence, slave read sequence
- Reset pins and configuration
- Utilization of the boot sequencer
- Requirement for an external Central Resource CPLD

IDMA CHANNELS

- IDMA address decoding
- Target unit and attributes programming
- Functional description, external control
- Normal mode vs chained mode
- Transfer descriptors, descriptor ownership
- Channel activation
- DMA interrupts

XOR ENGINES

- State machine : Active, Inactive and Paused states
- XOR, CRC and DMA operation modes, format of transfer descriptors
- XOR operation mode
- CRC32 operation mode
- DMA operation mode
- Memory Initialization operation mode
- ECC error cleanup operation mode
- Arbitration between XOR engine0 and XOR engine1
- Address override capability
- XOR Engines interrupts

16550 COMPATIBLE UARTs

- FIFO mode
- Flow control

- Transmit sequence
- Receive sequence

USB2.0 PORTS

- Address decoding
- Integrated PHY
- USB host operation, EHCI specification support
- USB device operation, Endpoint configuration
- Dedicated DMA for data movement between memory and port

SATA-II INTERFACE

- Integrated PHY, 3.0 or 1.5 Gbps bit rate
- EDMA request and response queues
- Studying the sequence that the software must implement to perform a PIO transfer
- Studying the sequence that the software must implement to perform a DMA transfer
- Queued DMA
- Interrupt coalescing
- Port multiplier support

GIGABIT ETHERNET CONTROLLERS

- SGMII support
- Dedicated DMA
- Related interrupts
- Transmit weighted round-robin arbitration
- Backpressure mode
- Transmit and receive sequences
- Management interface
- MIB

CRYPTOGRAPHIC ENGINE AND SECURITY ACCELERATORS

- Cryptographic engine functional description
- Involved units : CPU, dedicated SRAM and security accelerator
- Authentication
- Encryption and decryption, supported algorithms
- TDMA controller, attaching TDMA to security accelerator
- Multi-packet chained mode
- DES encryption / decryption sequence, pipelining

Renseignements pratiques

Durée : 5 jours
Prix : 2100 € HT