FCQ1 - P101X QorIQ implementation

This course covers NXP QorIQs P1010 & P1014

Objectives

- The course clarifies the architecture of the P1010 and P1014, particularly the operation of the coherency module that interconnects the e500 to memory and high-speed interfaces.
- Cache coherency protocol is introduced in increasing depth.
- The e500 core is viewed in detail, especially the SPE unit that enable vector processing.
- The boot sequence and the clocking are explained.
- The course focuses on the hardware implementation of the P101X.
- A long introduction to DDR SDRAM operation is done before studying the DDR3/3L SDRAM controller.
- An in-depth description of the PCI-Express port is done.
- The course explains how to implement QoS on GigaEthernet controllers.

- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- Performance for 1024 complex floating point single precision samples is:
  - - 91_386 core clock cycles without reverse ordering, 94_124 with reverse ordering
- Performance for 4096 complex floating point single precision samples is:
  - - 470_778 core clock cycles without reverse ordering, 511_227 with reverse ordering
- For any information contact training@ac6-training.com

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- Experience of a 32-bit processor or DSP is mandatory.
- The following courses could be of interest:
  - Ethernet and switching, reference cours N1 - Ethernet and switching
  - IEEE1588, reference cours N2 - IEEE1588 - Precise Time Protocol
  - PCI express gen2, reference cours IC4 - PCI Express 3.0
  - USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0
  - SD / MMC, reference cours IS2 - eMMC 5.0
  - Serial-ATA, reference cours IS3 - Serial ATA III
  - CAN bus, reference cours IA1 - CAN bus

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

INTRODUCTION TO P1010

SOC ARCHITECTURE

- Address map, ATMU, OCEAN configuration
- Local vs external address spaces, inbound and outbound address decoding
- Access control unit

THE e500 CORE

THE INSTRUCTION PIPELINE

- Dual-issue superscalar control, out-of-order execution
- Execution units
- Dynamic branch prediction
- Execution timing

DATA AND INSTRUCTION PATHS

- Load store unit, data buffering between LSU and CCB
- Store miss merging and store gathering
- Memory access ordering
- Lock acquisition and import barriers

THE MEMORY MANAGEMENT UNIT

- Thread vs process
- The first level MMU and the second level MMU, consistency between L1 and L2 TLBs
- TLB software reload, page attributes WIMGE
- Process protection, variable number of PID registers and sharing
- 36-bit real addressing

CACHES

- The L1 caches
- Level 2 cache, partition into L2 cache plus SRAM
- Snooping mechanism
- Stashing mechanism
- L2 cache locking
- ECC protection

PROGRAMMING

- Differences between the new Book E architecture and the classic PowerPC architecture
- Floating Point units, Double-Precision FP
- Signal Processing APU (SPU): implementation of the SIMD capability without using a separate unit
- PowerPC EABI: sections, C-to-assembly interface

EXCEPTIONS

- Critical versus non critical
- Handler table
- Syndrome registers
- Core timers

DEBUGGING

- Performance monitoring
- JTAG emulation
- Watchpoint logic

INFRASTRUCTURE

RESET, CLOCKING AND INITIALIZATION

- Voltage configuration selection
- Power-on reset sequence, using the I2C interface to access serial ROM
- Power-on reset configuration
- Power management
- Secure boot and trust architecture

e500 COHERENCY MODULE

- I/O arbiter
- CCB arbiter
- Global data multiplexor

DDR3/DDR3L SDRAM MEMORY CONTROLLER

- On-Die termination
- Calibration mechanism
- Mode registers initialization, bank selection and precharge
- Command truth table
- Bank activation, read, write and precharge timing diagrams, page mode
- Introduction to the DDR-SDRAM controller
- Initial configuration following Power-on-Reset
- Timing parameters programming

INTEGRATED FLASH CONTROLLER

- Functional muxing of pins between NAND, NOR, and GPCM
- Data Buffer Control
- Normal GPCM FSM
- NOR flash FSM
- Generic ASIC FSM
- NAND flash FSM

PCI EXPRESS INTERFACE

- 1-lane PCI Express interface
- Modes of operation, Root Complex / Endpoint
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Configuration, initialization

SATA CONTROLLER

- Electrical specification
- Native command queuing, command descriptor
- Interrupt coalescing
- Port multiplier operation
- Initialization steps

PROGRAMMABLE INTERRUPT CONTROLLER

- Interrupt sources
- Integrated timers
- Per-CPU register usage
- Nesting implementation

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency

PERFORMANCE MONITOR AND DEBUG FEATURES

- Event counting
- Threshold events
- Chaining, triggering
- Watchpoint facility
- Trace buffer

INPUTS/OUTPUTS

THE ETHERNET CONTROLLERS

- Address recognition, pattern matching
- Buffer descriptors management
- Physical interfaces: RGMII, SGMII
- Buffer descriptor management
- Layer 2 acceleration
- 256-entry hash table
- Direct queuing of four flows
- Management of VLAN
- Quality of service
- Filer programming
- IEEE1588 compliant time-stamping

TDM INTERFACE

- Hardware interface
- Program options for frame sync and clock generation
- Network mode of operation with up to 128 time-slots
- DMA configuration
- TDM power-down feature

- Configuring the TDM for I2S Operation

ENHANCED SECURE DEVICE HOST CONTROLLER

- Storing and executing commands targeting the external card
- Multi-block transfers
- Moving data by using the dedicated DMA controller
- Dividing large data transfers
- Card insertion and removal detection

USB CONTROLLER

- Dual-role (DR) operation
- EHCI implementation
- ULPI interfaces to the transceiver
- Dedicated DMA channels
- Endpoints configuration

SECURITY ENGINE

- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels
- Link tables
- XOR acceleration

FLEXCAN MODULES

- Message buffers, mask registers
- Time Stamp based on 16-bit free-running timer
- Short latency time due to an arbitration scheme for high-priority messages

LOW SPEED PERIPHERALS

- Description of the NS16552 compliant DUART
- I2C controllers
- Enhanced SPI

Renseignements pratiques

Durée : 5 jours
Prix : 2930 € HT